#23/E
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/875,501
Filing Date ..... June 4, 2001
Inventor ..... Klaus F. Schuegraf et al.
Assignee ..... Micron Technology, Inc.
Group Art Unit 2815
Examiner ..... E. Ortiz
Attorney's Docket No. MI22-1741
Title: Methods for Forming Wordlines, Transistor Gates, and Conductive Interconnects, and Wordline, Transistor Gate, and Conductive Interconnect Structures

RESPONSE TO MARCH 19, 2003 FINAL OFFICE ACTION ACCOMPANYING REQUEST FOR CONTINUED EXAMINATION (RCE)

To: Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

From: D. Brent Kenady
Tel. 509-624-4276; Fax 509-838-3424
Wells St. John P.S.
601 West First Avenue, Suite 1300
Spokane, WA 99201-3828

Responsive to the Final Office Action dated March 19, 2003, Applicant amends and remarks as follows:

AMENDMENTS

Underlines indicate insertions and ~~strikeouts~~ indicate deletions.